PROCESSOR

Publication number: JP11296345
Publication date: 1999-10-29
Inventor: WATANABE HIROMI; OKADA YUTAKA; NAKAMOTO TAKASHI; NAKASE JUNKO; NAKAGAWA TETSUYA
Applicant: HITACHI LTD
Classification:
- international: ***G06F7/00; G06F7/57; G06F7/575; G06F9/30; G06F15/78; H03K19/173;*** **G06F7/00; G06F7/48; G06F9/30; G06F15/76; H03K19/173;** (IPC1-7): G06F7/00; G06F15/78; H03K19/173
- European:
Application number: JP19980096124 19980408
Priority number(s): JP19980096124 19980408

Abstract of **JP11296345**

PROBLEM TO BE SOLVED: To provide a processor capable of reducing the circuit scale of an arithmetic and logic unit and dealing with the specification change of an arithmetic operation, and having the arithmetic and logic unit suited for executing a composite arithmetic operation. SOLUTION: In this processor 1, a programmable arithmetic and logic unit 14 is used for the arithmetic and logic unit part, and the inside part is constituted of plural variable logical blocks (or fixed logical blocks) arranged like a second-dimensional matrix and a variable signal line network for connecting them. The variable signal line network is constituted of plural horizontal signal lines, plural vertical signal lines, and plural switching matrixes for switching the connection. Then, wiring information for designating the logical structure of the plural variable logical blocks and the connecting operation of the variable signal line network in the programmable arithmetic unit 14 is preliminarily stored in a wiring information storing part in an arithmetic unit controller 15. At the time of executing an arithmetic operation demanded by a certain instruction, the wiring information stored corresponding to the arithmetic operation demanded by the instruction is read, and the programmable arithmetic unit 14 is changed to the arithmetic and logic unit for executing the arithmetic operation.